



STB60NF10 STP60NF10

N-CHANNEL 100V - 0.019 Ω - 80A D²PAK/TO-220 STripFET™ II POWER MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB60NF10	100 V	< 0.023 Ω	80 A
STP60NF10	100 V	< 0.023 Ω	80 A

- TYPICAL R_{DS(on)} = 0.019 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- SURFACE-MOUNTING D²PAK (TO-263) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH EFFICIENCY DC/DC CONVERTERS, INDUSTRIAL, AND LIGHTING EQUIPMENT.
- MOTOR CONTROL

Figure 1: Package

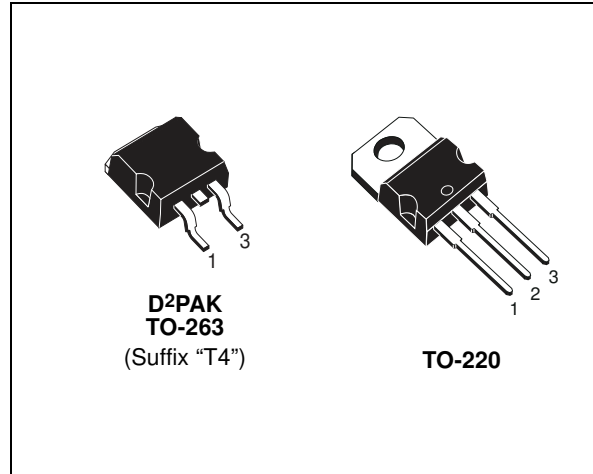


Figure 2: Internal Schematic Diagram

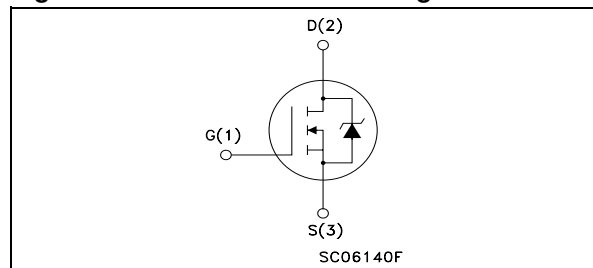


Table 2: Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STB60NF10T4	B60NF10	TO-263	TAPE & REEL
STP60NF10	P60NF10	TO-220	TUBE

Table 3: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	100	V
V _{GS}	Gate- source Voltage	\pm 20	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	66	A
I _{DM} (•)	Drain Current (pulsed)	320	A
P _{tot}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	16	V/ns
E _{AS} (2)	Single Pulse Avalanche Energy	485	mJ
T _{stg}	Storage Temperature	-55 to 175	°C

(•) Pulse width limited by safe operating area.

(**) Current Limited by Package

(1) I_{SD} \leq 80A, di/dt \leq 300A/ μ s, V_{DD} \leq V_{(BR)DSS}, T_j \leq T_{JMAX}

(2) Starting T_j = 25 °C, I_D = 40A, V_{DD} = 30V

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Table 4: THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose		300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

Table 5: OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

Table 6: ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 40 A		0.019	0.023	Ω

Table 7: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} = 25 V I _D = 40 A		78		S
C _{iss}	Input Capacitance	V _{DS} = 25V f = 1 MHz V _{GS} = 0		4270		pF
C _{oss}	Output Capacitance			470		pF
C _{rss}	Reverse Transfer Capacitance			140		pF

ELECTRICAL CHARACTERISTICS (continued)

Table 8: SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure)		17 56		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 50\text{ V}$ $I_D = 80\text{ A}$ $V_{GS} = 10\text{ V}$		104 20 32		nC nC nC

Table 9: SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 40\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		82 23		ns ns

Table 10: SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				80 320	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 80\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 80\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		92 340 7.4		ns μC A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (•) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

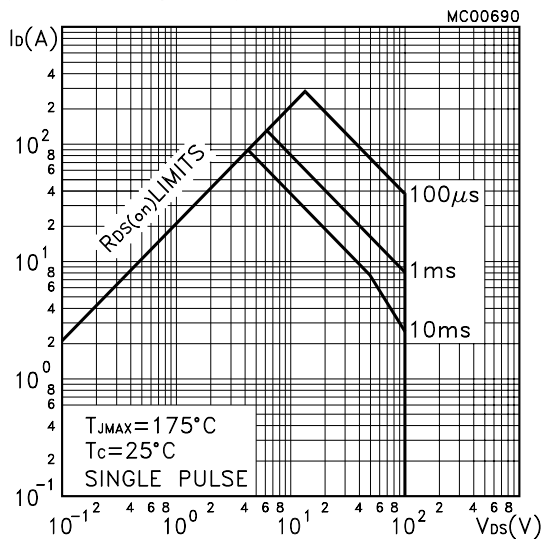


Figure 4: Thermal Impedance

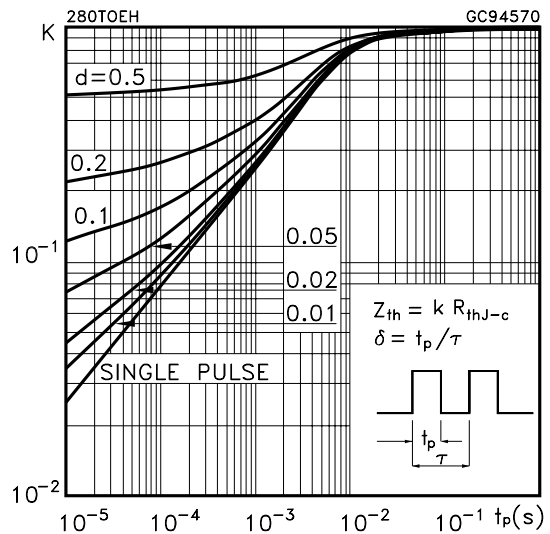


Figure 5: Output Characteristics

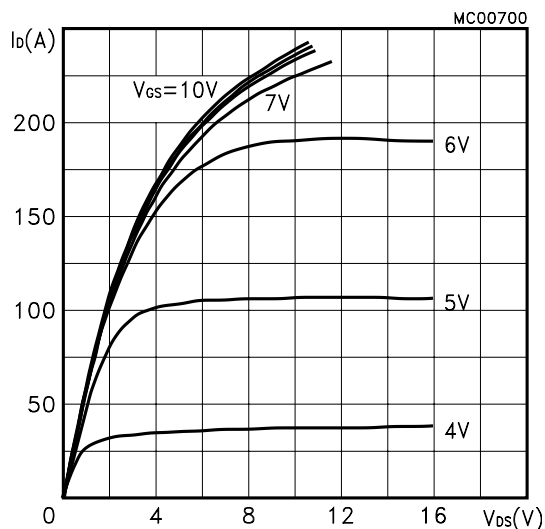


Figure 6: Transfer Characteristics

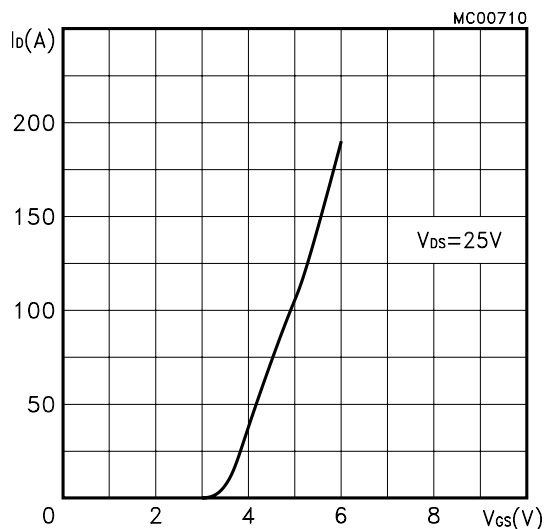


Figure 7: Transconductance

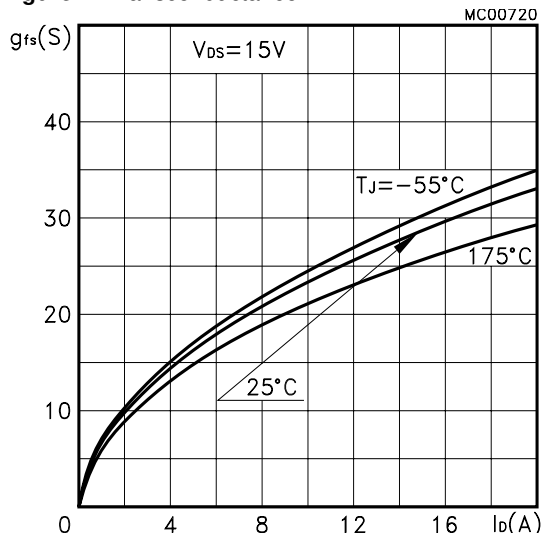


Figure 8: Static Drain-source On Resistance

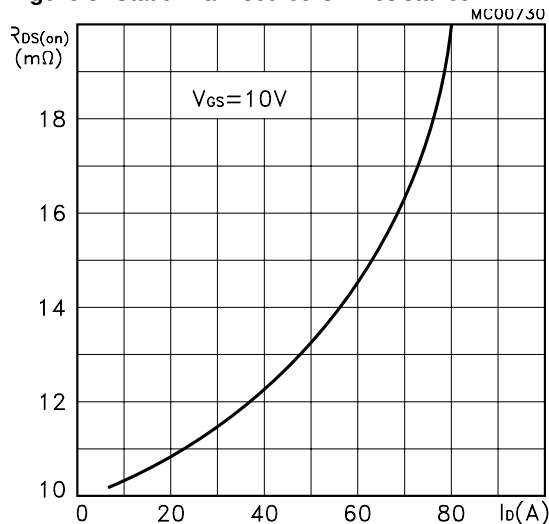


Figure 9: Gate Charge vs Gate-source Voltage

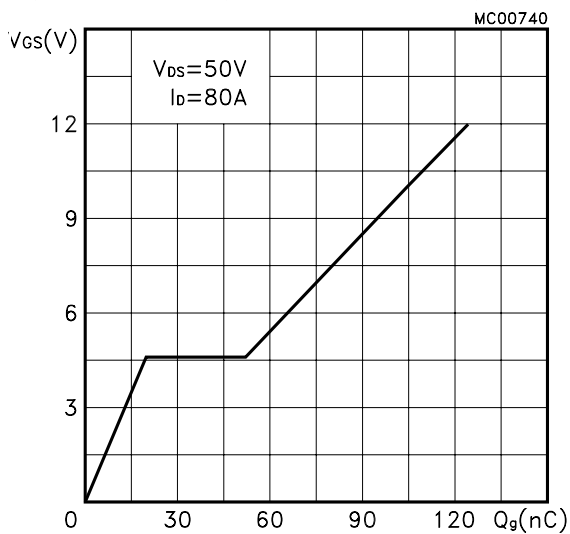


Figure 10: Capacitance Variations

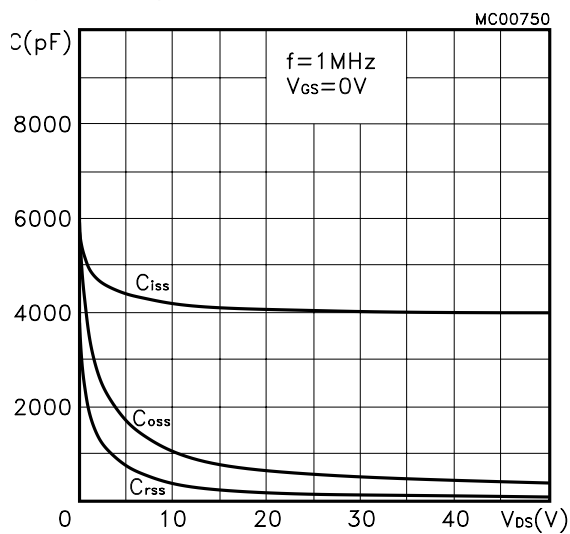


Figure 11: Normalized Gate Threshold Voltage vs Temperature

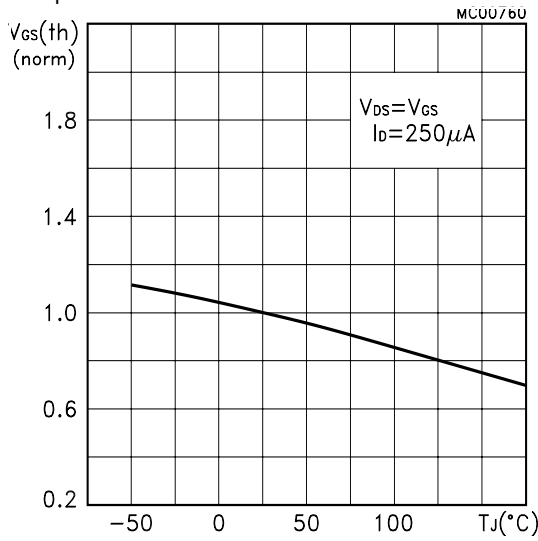


Figure 12: Normalized on Resistance vs Temperature

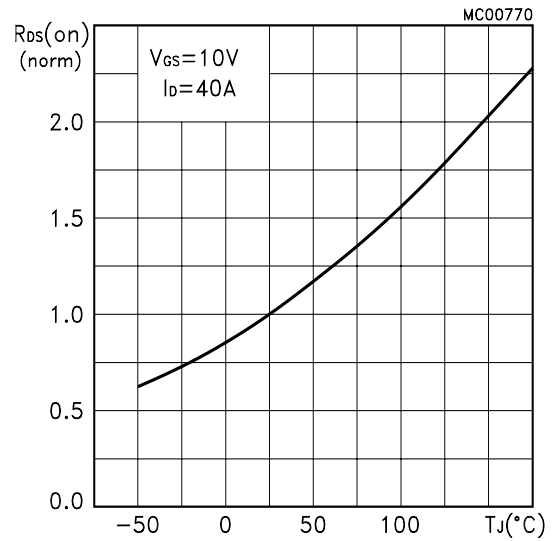


Figure 13: Source-drain Diode Forward Characteristics

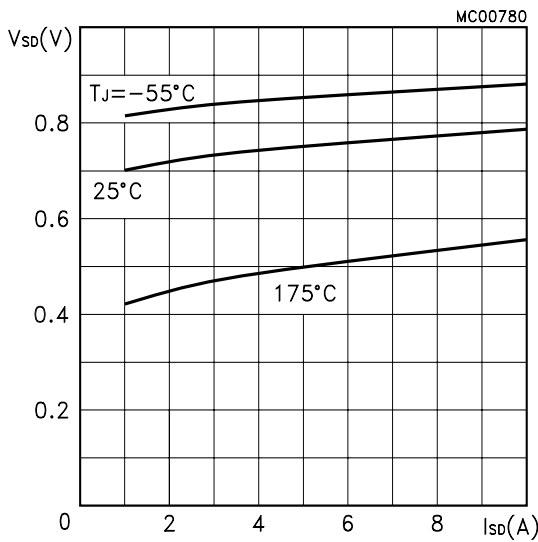


Figure 14: Normalized Breakdown Voltage vs Temperature.

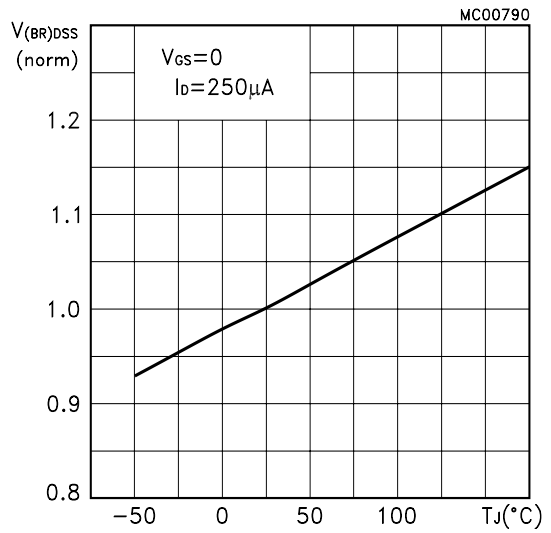


Figure 15: Unclamped Inductive Load Test Circuit

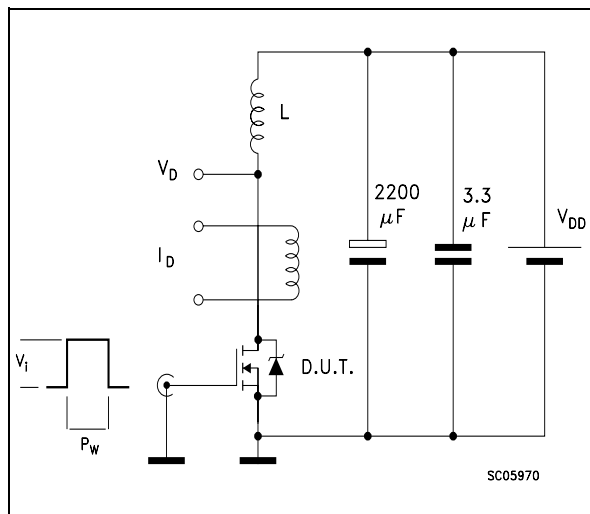


Figure 16: Unclamped Inductive Waveform

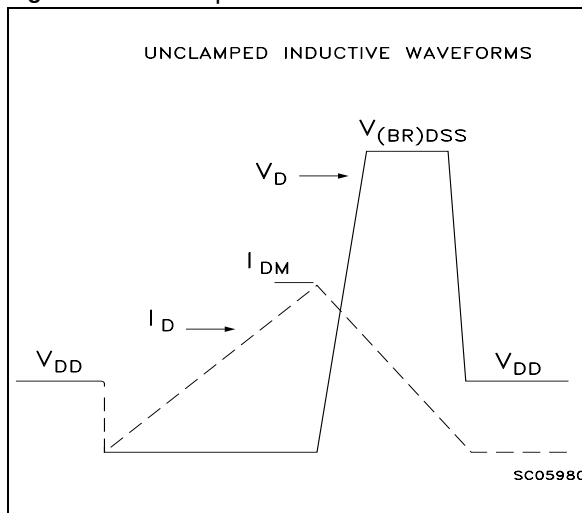


Figure 17: Switching Times Test Circuits For Resistive Load

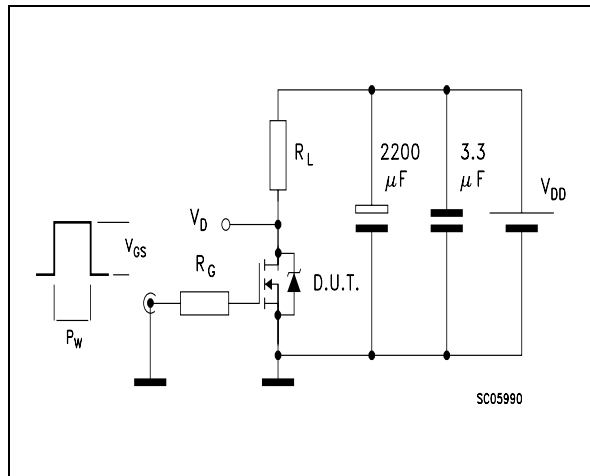


Figure 18: Gate Charge test Circuit

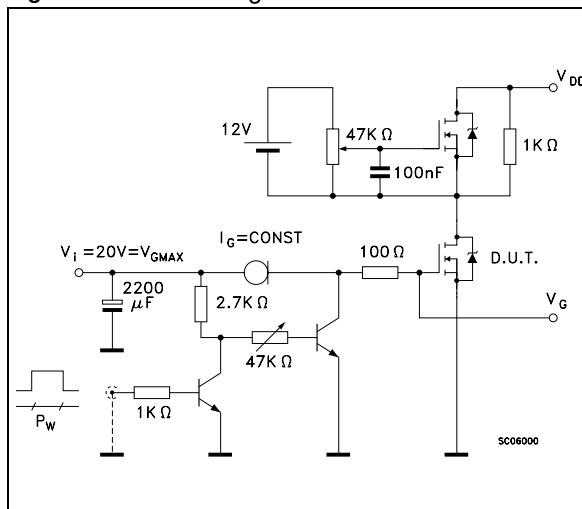
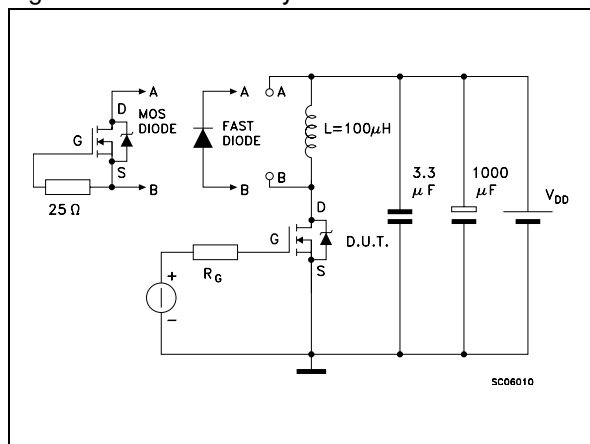
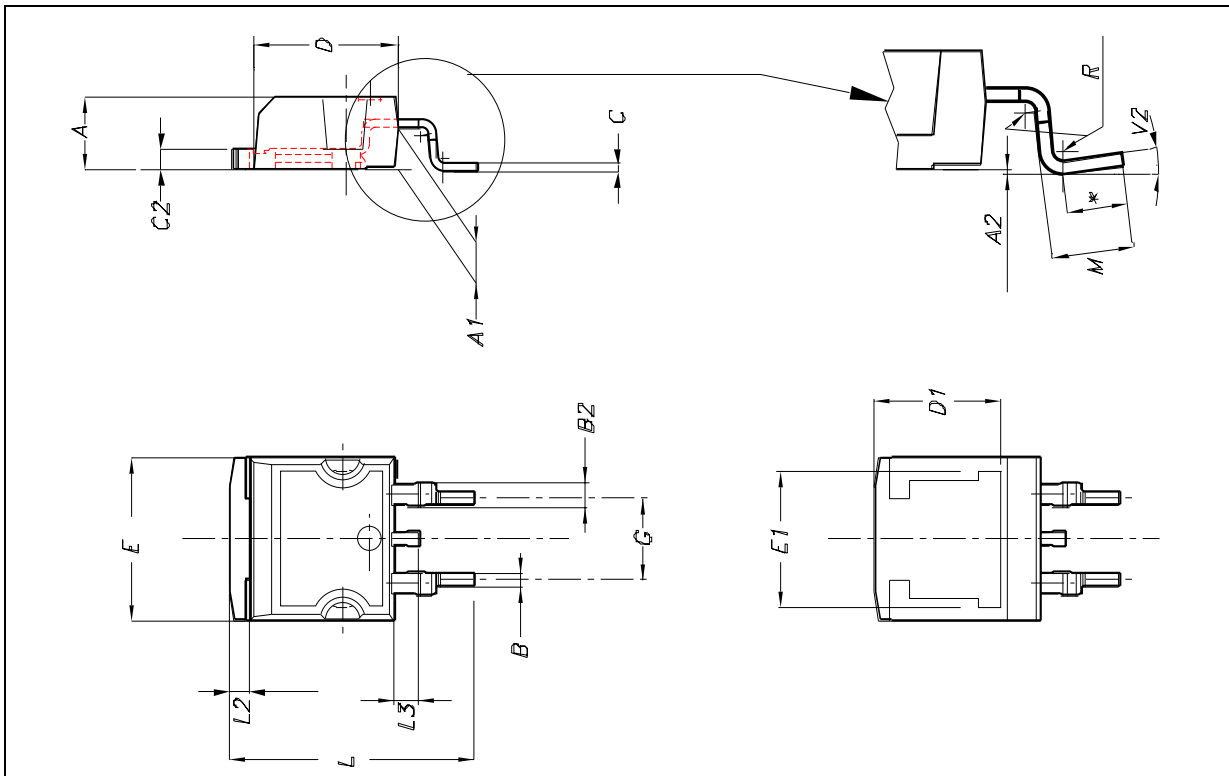


Figure 19: Test Circuit For Inductive Load Switching And Diode Recovery Times



D²PAK MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.028		0.037
B2	1.14		1.7	0.045		0.067
C	0.45		0.6	0.018		0.024
C2	1.21		1.36	0.048		0.054
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.394		0.409
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.591		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.069
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		8°	0°		8°



TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151

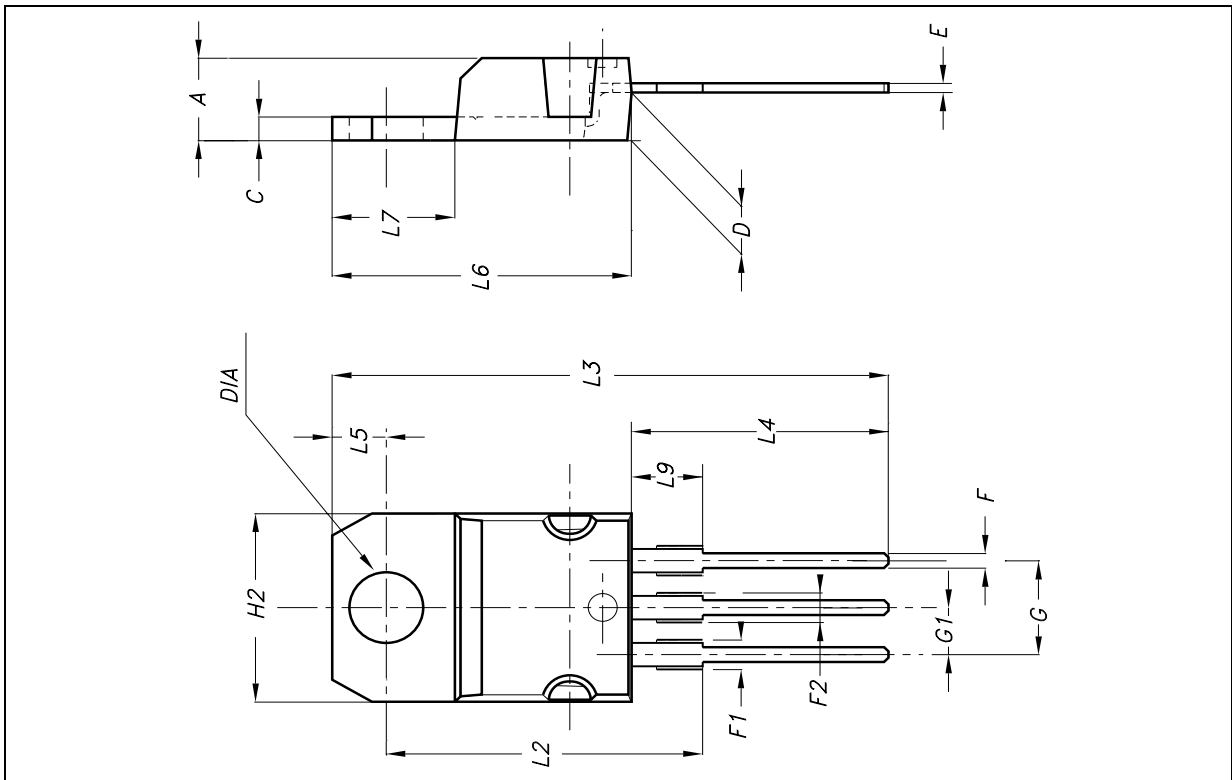


Table 11:Revision History

Date	Revision	Description of Changes
May 2005	1.0	FIRST ISSUE
May 2005	2.0	ADDED PACKAGE D ² PAK

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