MOTOROLA

Low Noise, JFET Input Operational Amplifiers

These low noise JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input device for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion, making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Low Input Noise Voltage: 18 nV/$\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: 10^{12} Ω Typ
- High Slew Rate: 13 V/μs Typ
- Wide Gain Bandwidth: 4.0 MHz Typ
- Low Supply Current: 1.4 mA per Amp

TL071C,AC
TL072C,AC
TL074C,AC

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

### SEMICONDUCTOR TECHNICAL DATA
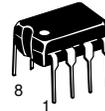
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

Offset Null	1	8 NC
Inv + Input	2	7 V_{CC}
Noninvt Input	3	6 Output
V_{EE}	4	5 Offset Null

TL071 (Top View)

Output A	1	8 V_{CC}
Inputs A	2	7 Output B
	3	6 Inputs B
V_{EE}	4	5

TL072 (Top View)
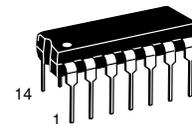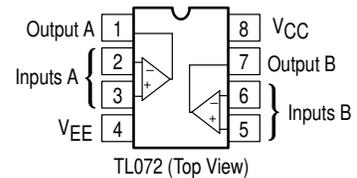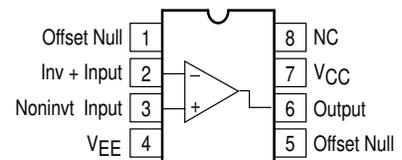
N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL074 Only)

PIN CONNECTIONS

Output 1	1	14 Output 4
Inputs 1	2	13 Inputs 4
	3	12
V_{CC}	4	11 V_{EE}
Inputs 2	5	10 Inputs 3
	6	9
Output 2	7	8 Output 3

TL074 (Top View)
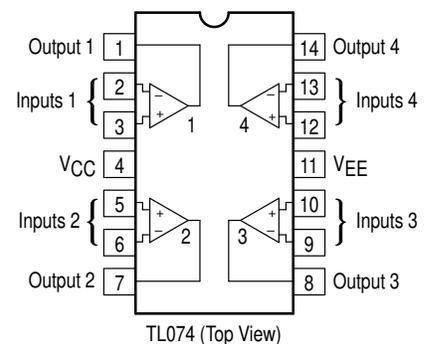
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL071CD	$T_A = 0°$ to $+70°C$	SO–8
	TL071ACP		Plastic DIP
Dual	TL072CD	$T_A = 0°$ to $+70°C$	SO–8
	TL072ACP		Plastic DIP
Quad	TL074CN, ACN	$T_A = 0°$ to $+70°C$	Plastic DIP

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Rev 1

TL071C,AC TL072C,AC TL074C,AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = 47°C	P_D $1.0/\theta_{JA}$	680 10	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
    2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.
    3. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 1])

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0) TL071C, TL072C TL074C TL07_AC	V_{IO}	 – – –	 – – –	 13 13 7.5	mV
Input Offset Current (V_{CM} = 0) (Note 2) TL07_C TL07_AC	I_{IO}	 – –	 – –	 2.0 2.0	nA
Input Bias Current (V_{CM} = 0) (Note 2) TL07_C TL07_AC	I_{IB}	 – –	 – –	 7.0 7.0	nA
Large–Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k) TL07_C TL07_AC	A_{VOL}	 15 25	 – –	 – –	V/mV
Output Voltage Swing (Peak–to–Peak) ($R_L \geq$ 10 k) ($R_L \geq$ 2.0 k)	V_O	 24 20	 – –	 – –	V

NOTES: 1. T_{low} = 0°C for TL071C,AC T_{high} = 70°C for TL071C,AC
               TL072C,AC   TL072C,AC
               TL074C,AC   TL074C,AC
    2. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

**Figure 1. Unity Gain Voltage Follower**
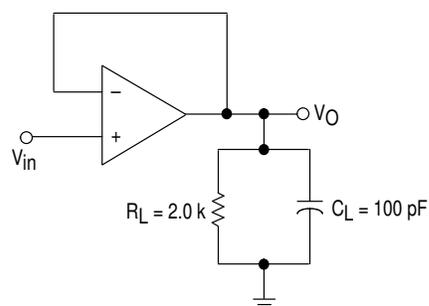

Figure 2. Inverting Gain of 10 Amplifier
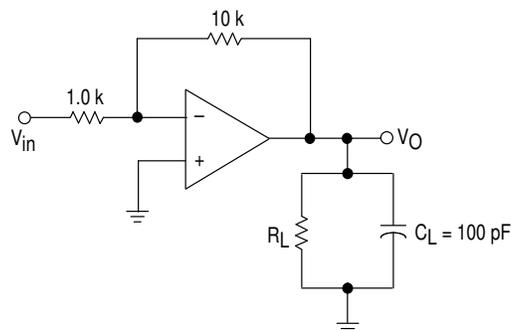
TL071C,AC TL072C,AC TL074C,AC

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit

Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0)
  TL071C, TL072C
  TL074C
  TL07_AC
	V_{IO}	
		−
		−
		−
			
			3.0
			3.0
			3.0
				
				10
				10
				6.0
					mV

Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 1)	$\Delta V_{IO}/\Delta T$	−	10	−	µV/°C

Input Offset Current (V_{CM} = 0) (Note 2)
  TL07_C
  TL07_AC
	I_{IO}	
		−
		−
			
			5.0
			5.0
				
				50
				50
					pA

Input Bias Current (V_{CM} = 0) (Note 2)
  TL07_C
  TL07_AC
	I_{IB}	
		−
		−
			
			30
			30
				
				200
				200
					pA

Input Resistance	r_i	−	10^{12}	−	Ω

Common Mode Input Voltage Range
  TL07_C
  TL07_AC
	V_{ICR}	
		±10
		±11
			
			15, −12
			15, −12
				
				−
				−
					V

Large–Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k)
  TL07_C
  TL07_AC
	A_{VOL}	
		25
		50
			
			150
			150
				
				−
				−
					V/mV

Output Voltage Swing (Peak–to–Peak) (R_L = 10 k)	V_O	24	28	−	V

Common Mode Rejection Ratio ($R_S \leq$ 10 k)
  TL07_C
  TL07_AC
	CMRR	
		70
		80
			
			100
			100
				
				−
				−
					dB

Supply Voltage Rejection Ratio ($R_S \leq$ 10 k)
  TL07_C
  TL07_AC
	PSRR	
		70
		80
			
			100
			100
				
				−
				−
					dB

Supply Current (Each Amplifier)	I_D	−	1.4	2.5	mA
Unity Gain Bandwidth	BW	−	4.0	−	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	−	13	−	v/µs
Rise Time (See Figure 1)	t_r	−	0.1	−	µs
Overshoot (V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF)	OS	−	10	−	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	−	18	−	nV/$\sqrt{\text{Hz}}$
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	−	0.01	−	pA/$\sqrt{\text{Hz}}$
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \leq$ 1.0 k, $R_L \geq$ 2.0 k, f = 1000 Hz	THD	−	0.01	−	%
Channel Separation A_V = 100	CS	−	120	−	dB

NOTES: 1. T_{low} = 0°C for TL071C,AC T_{high} = 70°C for TL071C,AC
              TL072C,AC   TL072C,AC
              TL074C,AC   TL074C,AC
     2. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

TL071C,AC TL072C,AC TL074C,AC

**Figure 3. Input Bias Current
versus Temperature**
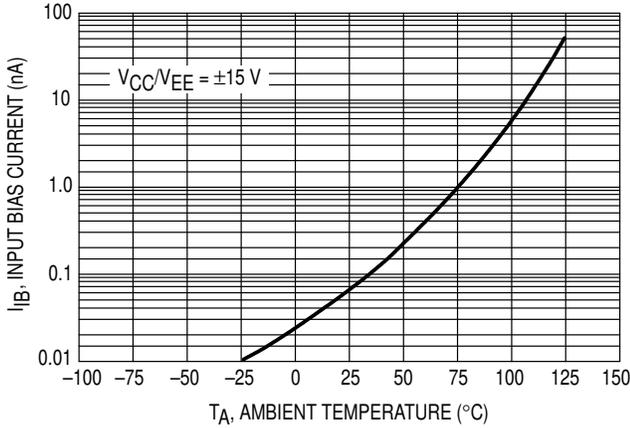
**Figure 4. Output Voltage Swing
versus Frequency**
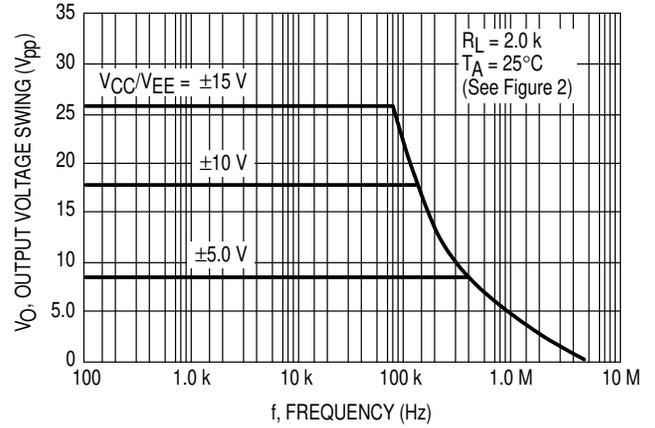
**Figure 5. Output Voltage Swing
versus Load Resistance**
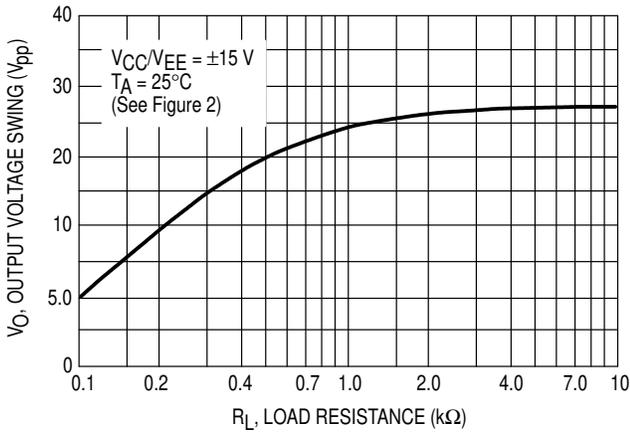

**Figure 6. Output Voltage Swing
versus Supply Voltage**
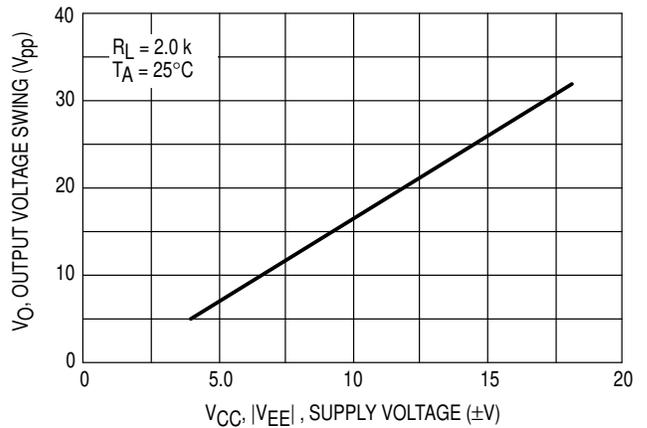

**Figure 7. Output Voltage Swing
versus Temperature**
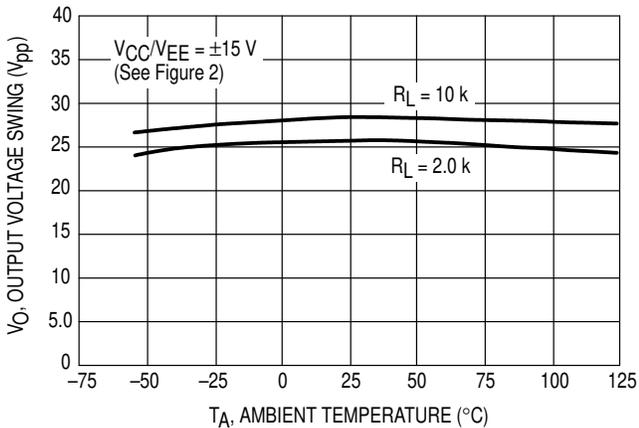
**Figure 8. Supply Current per Amplifier
versus Temperature**
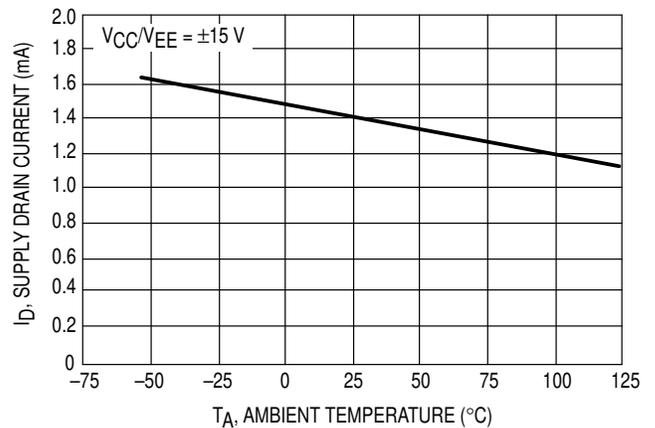
TL071C,AC TL072C,AC TL074C,AC

**Figure 9. Large Signal Voltage Gain and
Phase Shift versus Frequency**

$V_{CC}/V_{EE} = \pm 15$ V
$R_L = 2.0$ k
$T_A = 25°C$

Gain

Phase Shift
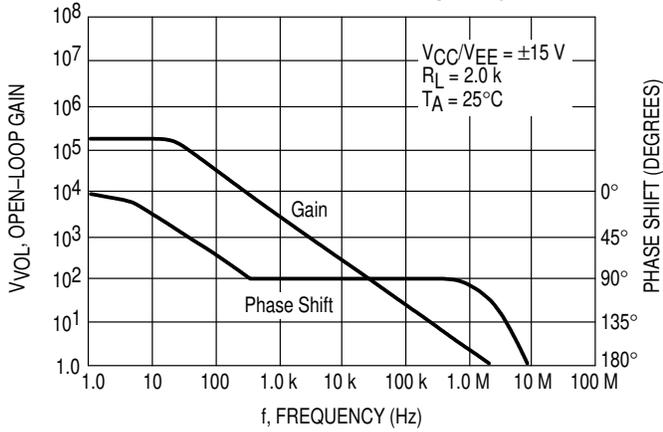
**Figure 10. Large Signal Voltage Gain
versus Temperature**

$V_{CC}/V_{EE} = \pm 15$ V
$V_O = \pm 10$ V
$R_L = 2.0$ k
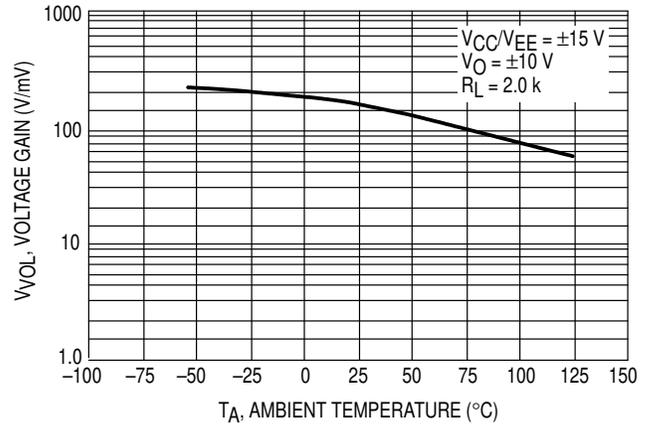
**Figure 11. Normalized Slew Rate
versus Temperature**
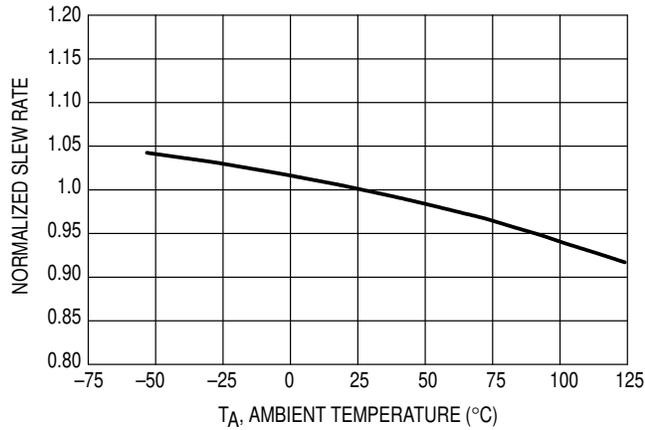
**Figure 12. Equivalent Input Noise Voltage
versus Frequency**

$V_{CC}/V_{EE} = \pm 15$ Vdc
$A_V = 10$
$R_S = 100$ Ω
$T_A = 25°C$
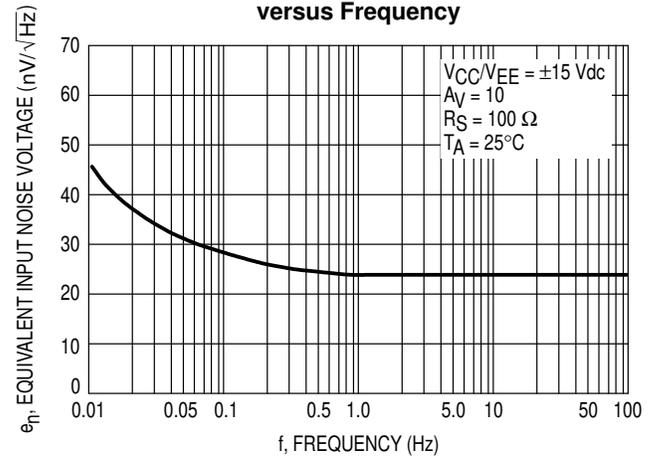
**Figure 13. Total Harmonic Distortion
versus Frequency**

$V_{CC}/V_{EE} = \pm 15$ V
$A_V = 1.0$
$V_O = 6.0$ V (RMS)
$T_A = 25°C$
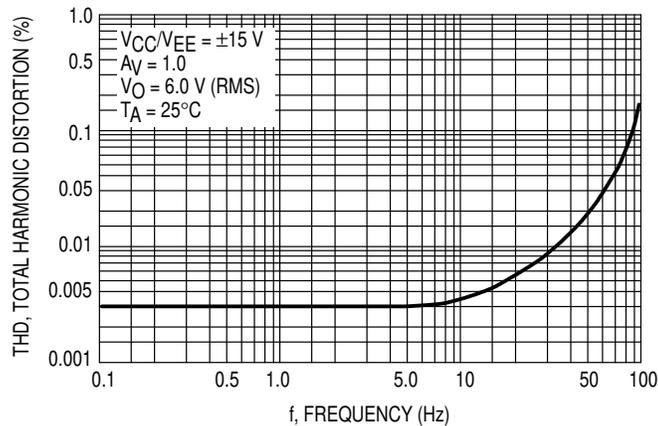
TL071C,AC TL072C,AC TL074C,AC

Representative Schematic Diagram

(Each Amplifier)
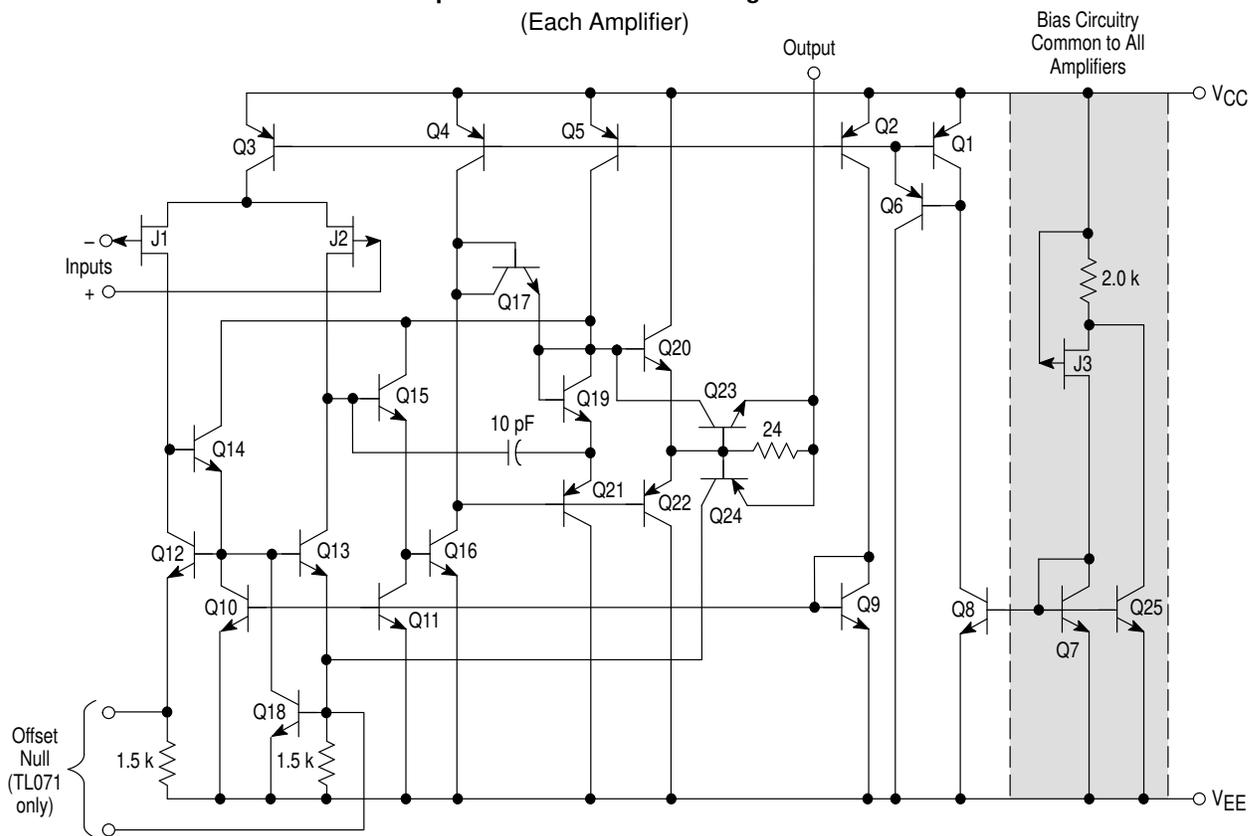
Figure 14. Audio Tone Control Amplifier

Turn–Over Frequency = 1.0 kHz
Bass Boost/Cut — ±20 dB at 20 Hz
Treble Boost/Cut — ±19 dB at 20 kHz
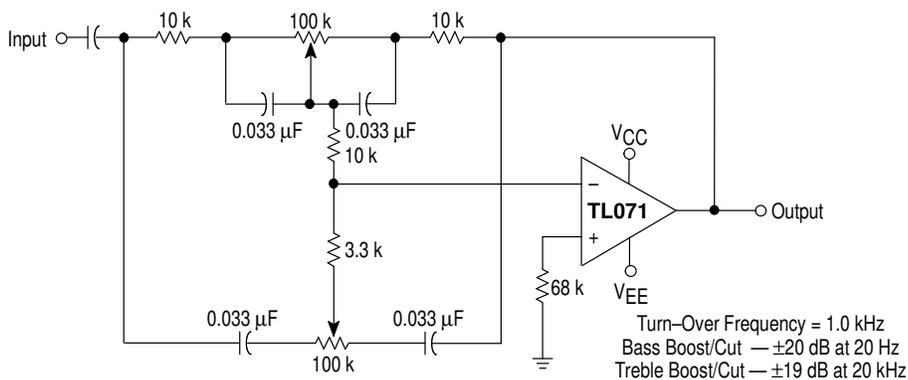
Figure 15. High Q Notch Filter

$$f_o = \frac{1}{2\pi RC} = 350 \text{ Hz}$$

$$R = 2R1 = 1.5 \text{ M}$$

$$C = \frac{C1}{2} = 300 \text{ pF}$$
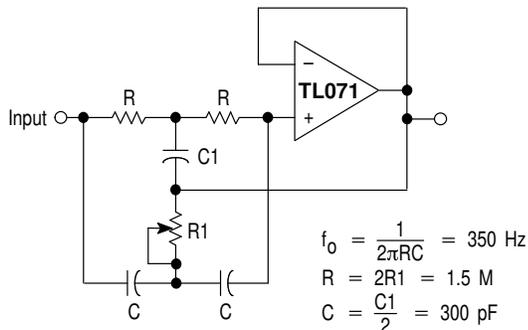
OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K

NOTE 2

–B–

–A–

F

C

–T–
SEATING
PLANE

N

D

K

H

G

L

J

M

$\oplus$ | $\varnothing$ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
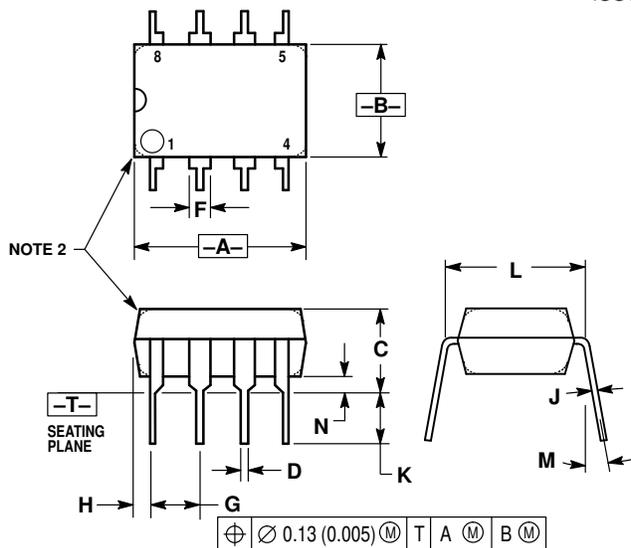
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE S

A

D

E

H

B

e

$\oplus$ | 0.25 Ⓜ | B Ⓜ

C

h X 45°

θ

L

C

A

SEATING
PLANE

$\cap$ | 0.10

A1

B

$\oplus$ | 0.25 Ⓜ | C | B Ⓢ | A Ⓢ
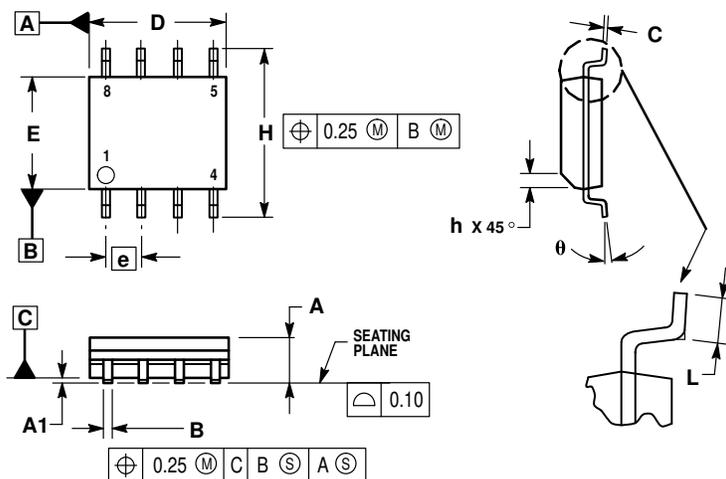
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE M

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
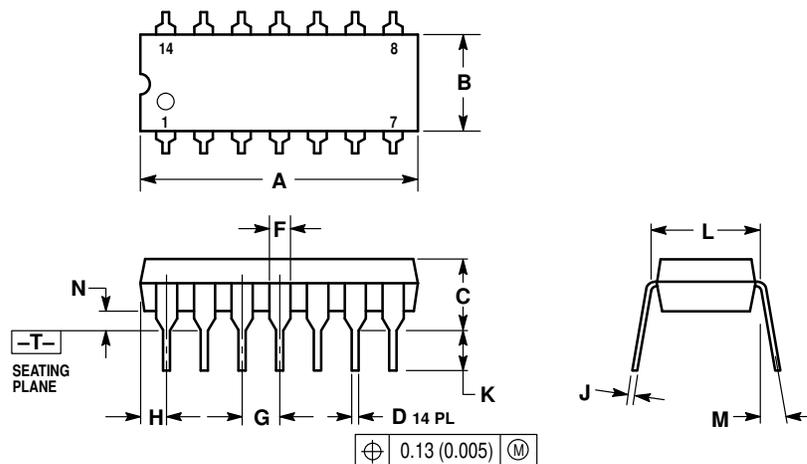
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—	10°	—	10°
N	0.015	0.039	0.38	1.01

⊕ | 0.13 (0.005) | Ⓜ

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