

KATHREIN

SHANGHAI SAMSUNG SVA ELECTRONICS
 DEVICES CO., LTD. VFD DEVELOPMENT
 TEL : 86-21-5774-6000(Extension NO. : 5800~5807)
 DESIGNER : TANG YINGTING



VFD SALES PART (CHINA)
 TEL : 86-21-5774-6000(Extension NO. : 8000~8010)
 FAX : 86-21-5774-2244

SPECIFICATION

STB

VACUUM FLUORESCENT DISPLAY

HCS-12SS59T

	Date	Descriptions	Approved by
1	2009.04.22	Refer to REVISION RECORD	/
2			
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Designed by	Checked by	Approved by
 04/22	 04.22	 17.22

Customer's Approval

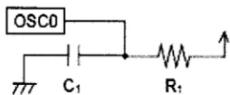
Pin Description

Pin Name	I/O	Description
F+,F-	-	Filament Voltage
V _{DD}	-	V _{DD} -GND are Power Supplies for Internal logic V _{EE} -GND are Power Supplies for driving CIG VFD. (Note: Apply V _{EE} after V _{DD} is applied)
GND		
V _{EE}		
OSC0	I/O	Oscillator
$\overline{\text{RST}}$	I	Reset Input : When RST is set to "LOW", all functions are initialized.
$\overline{\text{CS}}$	I	Chip Select Input : When CS is set to "HIGH", the serial data transfer is disabled.
CLK	I	Shift Clock Input : The serial data is shifted at the rising edge of CLK
DIN	I	Serial Data Input

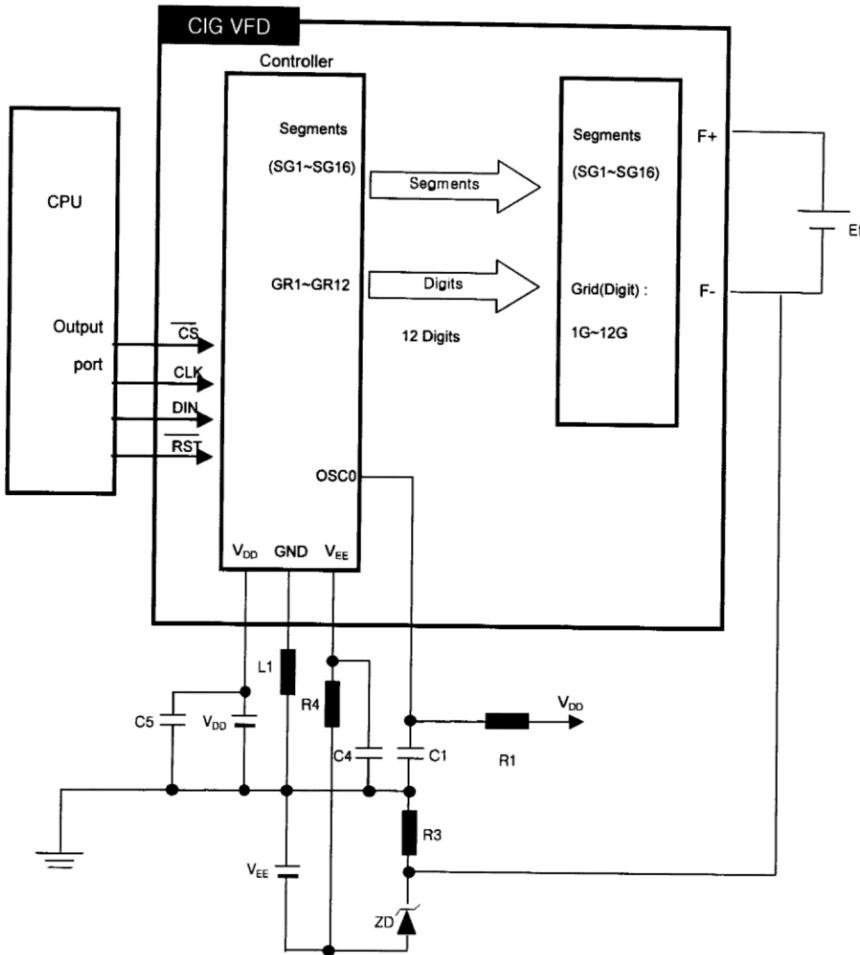
Oscillation Circuit

An oscillation circuit may be constructed by connecting external Resistor (R1) and Capacitor (C1) between the oscillator pin -- OSC0. The RC time constant depends on the value of V_{DD} voltage used.

The target oscillation frequency is 2MHz. Please refer to the diagram below.



Application Circuit



「Note」

Passive components relating oscillation and reset are required to be located as close as possible to VFD.

- R4 : Current Limiting Resistor (470Ω)
- L1 : Bead(Inductor) for improving ESD ... CIC21J601NE(Maker:SEM) equivalent
- C4 : Bypass Capacitor for High Voltage (0.1uF, 60V)
- C5 : Bypass Capacitor for Logic Voltage (0.1uF)

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage_1	V _{DD}	-	-0.3 to 6.5	V _{DC}
Supply Voltage_2	V _{EE}	-	-0.3~+45.0	V _{DC}
Input Voltage	V _{IN}	-	-0.3 to V _{DD} +0.3	V _{DC}
Storage Temperature	T _{STG}	-	-55 to +85	°C

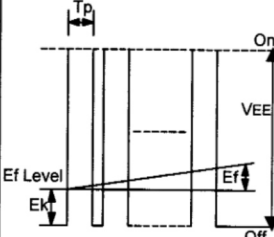
Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Filament Voltage	E _f	-	3.24	3.6	3.96	V _{DC}
Supply Voltage_1	V _{DD}	-	4.5	5.0	5.5	V _{DC}
Supply Voltage_2	V _{EE}	-	30.6	34.0	37.4	V _{DC}
High Level Input Voltage	V _{IH}	All Input pins except OSC0	0.7 V _{DD}	-	-	V _{DC}
Low Level Input Voltage	V _{IL}	All Input pins except OSC0	-	-	0.3 V _{DD}	V _{DC}
Cut-off Voltage	E _k	-	2.0	-	-	V _{DC}
CLK Frequency	f _C	-	-	-	2.0	MHz
Oscillation Frequency	f _{OSC}	R1=8.2kΩ, C1=82pF	1.4	2.0	2.6	MHz
Frame Frequency	f _{FR}	R1=8.2kΩ, C1=82pF	170	244	318	Hz
Operating Temperature	T _{OPR}	-	-20	-	+70	°C

DC Electrical Characteristics

Parameter	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
High Level Input Voltage	V _{IH}	CS, CLK, DIN, RST	-	0.7 V _{DD}	-	-	V _{DC}
Low Level Input Voltage	V _{IL}	CS, CLK, DIN, RST	-	-	-	0.3 V _{DD}	V _{DC}
High Level Input Current	I _{IH}	CS, CLK, DIN, RST	V _{IH} =V _{DD}	-1.0	-	1.0	μA
Low Level Input Current	I _{IL}	CS, CLK, DIN, RST	V _{IL} =0.0V	-1.0	-	1.0	μA
High Level Output Voltage	V _{OH1}	COM1~16	I _{OH} =-30mA	V _{DISP} -1.5	-	-	V _{DC}
	V _{OH2}	AD1~2	I _{OH} =-15mA	V _{DISP} -1.5	-	-	V _{DC}
	V _{OH3}	SEG1~16	I _{OH} =-6mA	V _{DISP} -1.5	-	-	V _{DC}
Low Level Output Voltage	V _{OL}	-	-	-	1.0	V _{DC}	
Filament Current	I _f	F+ and F-	V _{DD} =V _{EE} =Open	113	125	138	mA
Current Consumption	I _{DD} (Peak)	-	-	-	13	26	mA
	I _{DD} (AVE)	-	-	-	11	22	mA

Optical Characteristics

ITEMS	Test Conditions	Color	Min.	Typ.	Max.	Unit
Brightness	$E_f = 3.60$ Vdc	GREEN	102	204	—	ft-L
	$V_{DD} = 5.0$ Vdc					
	$V_{EE} = 34.0$ Vdc					
	$E_K = 2.0$ Vdc					
	$f_{osc} = 2.0$ MHz					
Brightness Ratio Between Digits	$T_p = 240$ μ s	$\frac{L(\text{Max})}{L(\text{Min})}$	-	-	2	-
	$T_b = 16$ μ s					
Color Coordinate NOTE 1)	 <p>The diagram shows a timing sequence for the optical characteristics. It includes a clock signal (CLK) with period T_p and pulse width T_b. The E_f level is shown as a horizontal line, and the E_k level is shown as a vertical line. The On signal is shown as a pulse, and the VEE signal is shown as a pulse. The Off signal is shown as a pulse. The color coordinate is GREEN (G. :x=0.250,y=0.439).</p>	GREEN (G. :x=0.250,y=0.439)				

NOTE 1. All phosphor is Cd-free phosphor.

AC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Max.	Unit
CLK Cycle Time	f_c	-	-	2.0	MHz
CLK Pulse Width	t_{CW}	-	250	-	ns
DIN Setup Time	t_{DS}	-	250	-	ns
DIN Hold Time	t_{DH}	-	250	-	ns
CS Setup Time	t_{CSS}	-	250	-	ns
CS Hold Time	t_{CSH}	$R1=8.2k\Omega, C1=82pF$	16	-	μ s
CS Wait Time	t_{CSW}	-	250	-	ns
Data Processing Time	t_{DOFF}	$R1=8.2k\Omega, C1=82pF$	8	-	μ s
RST Pulse Width	t_{WRST}	When RST Signal is input from microcontroller etc. externally	250	-	ns
RST Time	t_{RSON}	-	250	-	ns
D_{IN} Wait Time	t_{RSOFF}	-	250	-	ns
All Output Slew Rate	t_R	$CI=100pF, tR=20\%$ to 80%	-	2.0	μ s
	t_F	$CI=100pF, tF=80\%$ to 20%	-	2.0	μ s

Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer. Write timing is shown in the figure below.

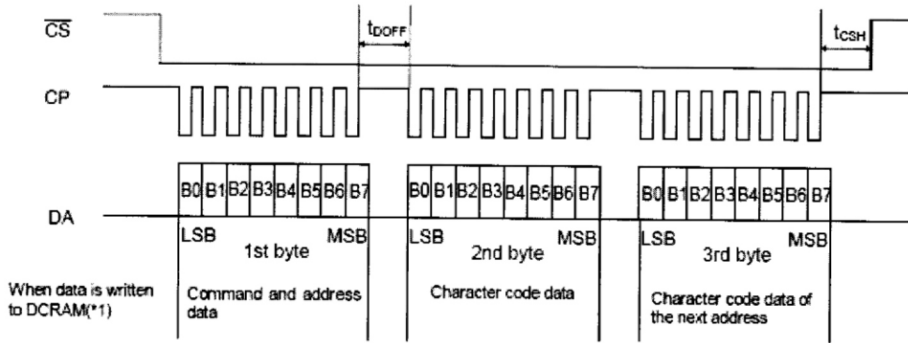
Setting the CS pin to "Low" level enables a data transfer.

Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).

As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the CP pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.

Therefore it is not necessary to input load signals from the outside.

Setting the CS pin to "High" disables data transfer. Data input from the point when the CS pin changes from "High" to "Low" is recognized in 8-bit units.



*1 When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and subsequent bytes.

Reset Function

Reset is executed when the RESET pin is set to "L", (when turning power on, for example) and initializes all functions.

Initial status is as follows.

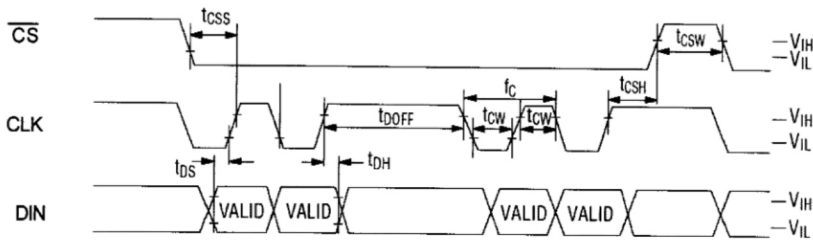
- Address of each RAM..... Address 00H
- Data of each RAM..... All contents are undefined.
- Number of display digits..... 16 digits
- Brightness adjustment..... 0/16
- All display lights ON or OFF..... OFF mode
- Segment output..... All segment outputs go "Low."
- AD output..... All AD outputs go "Low."

Be sure to execute the reset operation when turning power on and set again according to "Setting Flowchart" after reset.

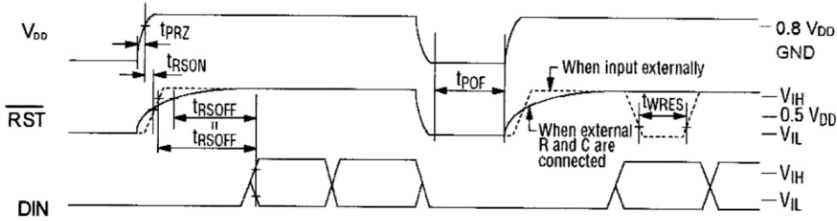
Timing Characteristics

Parameter	Symbol	$V_{DD} = 5.0 \pm 10\%$
High Level Input Voltage	V_{IH}	$0.7 V_{DD}$
Low Level Input Voltage	V_{IL}	$0.3 V_{DD}$

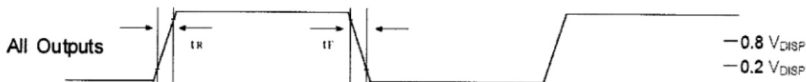
- Data TIMING



- Reset Timing



- Output Timing



Note: 14 SEG Mode was initially fixed, so SEG2 and SEG5 will not be connected.
 For 16, 14, 7 SEG MODE, please find the detailed FONT-MAP in page 19.

Command List

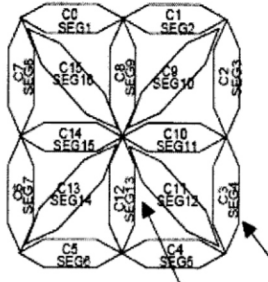
Command	First byte							Second byte								
	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
1 DCRAM data write	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7
2 CGRAM data write	X0	X1	X2	X3	0	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7
									C8	C9	C10	C11	C12	C13	C14	C15
3 ADRAM data write	X0	X1	X2	X3	1	1	0	0	C0	C1	*	*	*	*	*	*
4 Display duty set	D0	D1	D2	D3	1	0	1	0								
5 Number of digits set	K0	K1	K2	K3	0	1	1	0								
6 All display lights ON/OFF	L	H	*	*	1	1	1	0								
Others (test mode)																

* : Don't care
 Xn : Address setting for each RAM
 Cn : Character code setting for each RAM
 Dn : Display duty setting
 Kn : Setting of the number of display digits
 H : All display lights ON setting
 L : All display lights OFF setting

When data is written to RAM (DCRAM, CGRAM, and ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and subsequent bytes.

Note: The test mode is used for inspection before shipment. It is not a user function.

Positional Relationship Between SEGn and ADn (one digit)



Note

C0-7: Corresponds to the 2nd byte of the CGRAM data write command.

C8-15: Corresponds to the 3rd byte of the CGRAM data write command.

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
C0	C1	C2	C3	C4	C5	C6	C7
SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
C8	C9	C10	C11	C12	C13	C14	C15

Note: SEG2 and SEG5 herein are suspended with no connection, therefore both "0" or "1" level in bit C1 and C4 could be acceptable.

Description of Commands and Functions

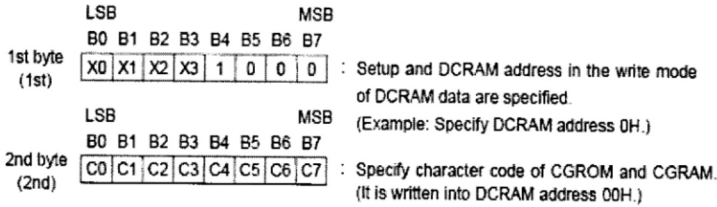
1. "DCRAM data write" command

(Specifies the address of DCRAM and writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 4-bit address to store character codes of CGROM and CGRAM. A character code specified by DCRAM is converted to an alphanumeric character pattern via CGROM or CGRAM.

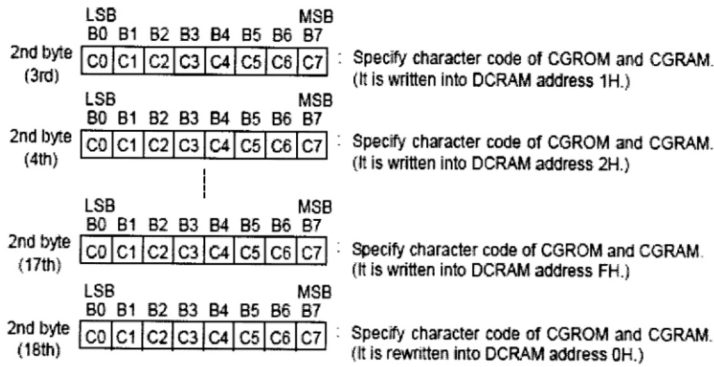
The DCRAM can store 16 characters worth of character codes.

[Command format]



To specify the character code of CGROM and CGRAM to the next address continuously, specify only character code as follows.

Since the address of DCRAM is automatically incremented, address specification is unnecessary.



X0 (LSB) to X3 (MSB): DCRAM address (4 bits: 16 characters worth)

C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 characters worth)

[Positional relationship between CGRAM addresses setup and CGROM addresses]

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
0	0	0	0	0	RAM00	8	0	0	0	1	RAM08
1	1	0	0	0	RAM01	9	1	0	0	1	RAM09
2	0	1	0	0	RAM02	A	0	1	0	1	RAM0A
3	1	1	0	0	RAM03	B	1	1	0	1	RAM0B
4	0	0	1	0	RAM04	C	0	0	1	1	RAM0C
5	1	0	1	0	RAM05	D	1	0	1	1	RAM0D
6	0	1	1	0	RAM06	E	0	1	1	1	RAM0E
7	1	1	1	0	RAM07	F	1	1	1	1	RAM0F

2. "CGRAM data write" command
(Specifies the address of CGRAM and writes character pattern data.)

CGRAM (Character Generator RAM) has a 4-bit address to store alphanumeric character patterns. A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM. The addresses of CGRAM are assigned to 00H to 0FH (All the other addresses are the CGROM addresses). The CGRAM can store 16 types of character patterns.

[Command format]

1st byte (1st)

LSB				MSB			
B0	B1	B2	B3	B4	B5	B6	B7
X0	X1	X2	X3	0	1	0	0

 : Setup and CGRAM address in the write-in mode of CGRAM data are specified.
(Example: Specify CGRAM address 00H.)

Note 2nd byte (2nd)

LSB				MSB			
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

 : Specify 1st-column data.
(It is written into CGRAM address 00H.)

3rd byte (3rd)

LSB				MSB			
B0	B1	B2	B3	B4	B5	B6	B7
C8	C9	C10	C11	C12	C13	C14	C15

 : Specify 2nd-column data.
(It is written into CGRAM address 00H.)

To specify character pattern data continuously to the next address, specify only character pattern data as follows. Since the address of CGRAM is automatically incremented, address specification is unnecessary. Data from the 2nd to 6th byte (character pattern) is regarded as one data item taken together, so 8 μ s is sufficient for t_{OFF} time between bytes.

Note 2nd byte (4th)

LSB				MSB			
B0	B1	B2	B3	B4	B5	B6	B7
C0	C1	C2	C3	C4	C5	C6	C7

 : Specify 1st-column data.
(It is written into CGRAM address 01H.)

3rd byte (5th)

LSB				MSB			
B0	B1	B2	B3	B4	B5	B6	B7
C8	C9	C10	C11	C12	C13	C14	C15

 : Specify 2nd-column data.
(It is written into CGRAM address 01H.)

X0 (LSB) to X3 (MSB): CGRAM address (4 bits: 16 characters worth)
C0 (LSB) to C15 (MSB): Character data of CGRAM (16 bits: 16 outputs per digit)

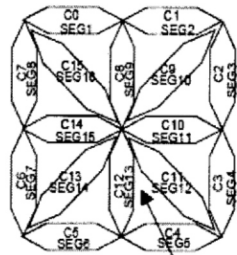
Note: Bit C1 and C4 in 2nd byte means suspended terminal SEG2 and SEG5. Therefore both "0" or "1" level in bit C1 and C4 could be acceptable.

[Positional relationship between CGRAM addresses setup and CGROM addresses]

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
0	0	0	0	0	RAM00	8	0	0	0	1	RAM08
1	1	0	0	0	RAM01	9	1	0	0	1	RAM09
2	0	1	0	0	RAM02	A	0	1	0	1	RAM0A
3	1	1	1	0	RAM03	B	1	1	0	1	RAM0B
4	0	0	1	0	RAM04	C	0	0	1	1	RAM0C
5	1	0	1	0	RAM05	D	1	0	1	1	RAM0D
6	0	1	1	0	RAM06	E	0	1	1	1	RAM0E
7	1	1	1	0	RAM07	F	1	1	1	1	RAM0F

Refer to the ROM Code Tables attached later in this document.

Positional Relationship Between CGROM and CGRAM outputs



Note

C0-7: Corresponds to the 2nd byte of the CGRAM data write command.

C8-15: Corresponds to the 3rd byte of the CGRAM data write command.

***On CGROM**

A CGROM (Character Generator ROM) has an 8-bit address to generate alphanumeric type matrix character patterns.

It has a capacity of 240 x 16 bits and can store 240 types of character patterns.

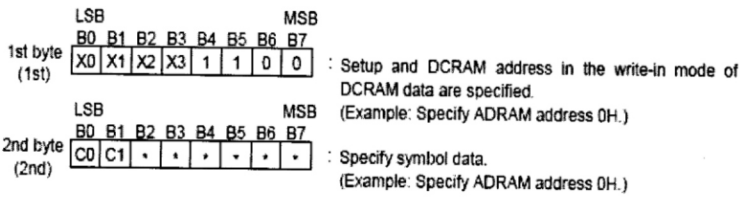
SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
C0	C1	C2	C3	C4	C5	C6	C7
SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
C8	C9	C10	C11	C12	C13	C14	C15

Note: Bit C1(SEG2) and C4(SEG5) would be required in data process even in fixed 14-Seg Mode. However, both "0" or "1" would be acceptable.

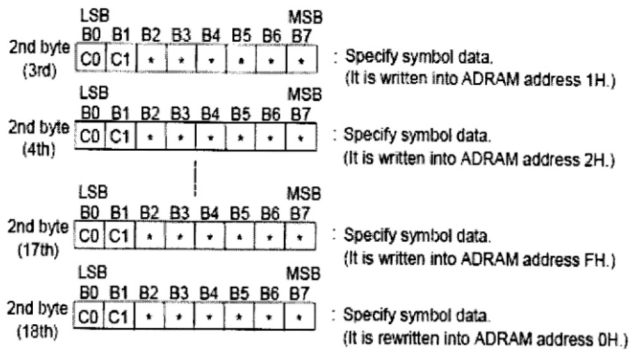
3. "ADRAM data write" command
(Specifies the address of ADRAM and writes symbol data)

ADRAM (Additional Data RAM) has a 2-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store two types of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

[Command format]



To specify symbol data continuously to the next address, specify only symbol data as follows.
Since the address of ADRAM is automatically incremented, address specification is unnecessary.



X0 (LSB) to X3 (MSB) : ADRAM address (4 bits: 16 characters worth)
C0 (LSB) to C1 (MSB) : Symbol data (2 bits: 2 symbols per digit)
* : Don't care

[Relationship between ADRAM addresses setup and COM positions]

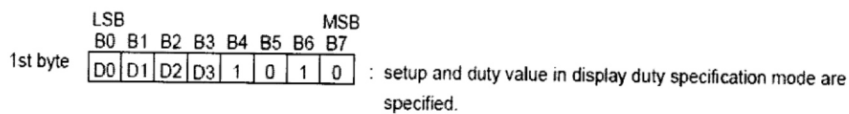
HEX	X0	X1	X2	X3	COM positions	HEX	X0	X1	X2	X3	COM positions
0	0	0	0	0	COM1	8	0	0	0	1	COM9
1	1	0	0	0	COM2	9	1	0	0	1	COM10
2	0	1	0	0	COM3	A	0	1	0	1	COM11
3	1	1	1	0	COM4	B	1	1	0	1	COM12
4	0	0	1	0	COM5	C	0	0	1	1	COM13
5	1	0	1	0	COM6	D	1	0	1	1	COM14
6	0	1	1	0	COM7	E	0	1	1	1	COM15
7	1	1	1	0	COM8	F	1	1	1	1	COM16

4. "Display duty set" command
(Writes display duty value into the duty cycle register.)

For display duty, brightness can be adjusted in 16 stages using 4-bit data.

When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this command before turning the display on, then set a desired duty value.

[Command format]



D0 (LSB) to D3 (MSB) : Display duty data (4 bits: 16 stages worth)

[Relation between setup data and controlled COM duty]

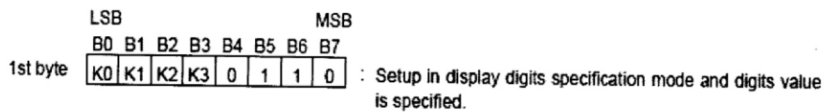
HEX	D0	D1	D2	D3	COM duty	HEX	D0	D1	D2	D3	COM duty
0	0	0	0	0	0/16	8	0	0	0	1	8/16
1	1	0	0	0	1/16	9	1	0	0	1	9/16
2	0	1	0	0	2/16	A	0	1	0	1	10/16
3	1	1	0	0	3/16	B	1	1	0	1	11/16
4	0	0	1	0	4/16	C	0	0	1	1	12/16
5	1	0	1	0	5/16	D	1	0	1	1	13/16
6	0	1	1	0	6/16	E	0	1	1	1	14/16
7	1	1	1	0	7/16	F	1	1	1	1	15/16

* The state when power is turned on or when the RESET signal is input.

5. "Number of display digits set" command
 (Writes the number of display digits into the number-of-display-digits register.)

For the number of display digits, 1 to 16 digits can be specified using 4-bit data.
 When power is turned on or when a RESET signal is input, the number-of-display-digits register value is "0".
 Always execute this command before turning the display on, then set a desired value.

[Command format]



K0 (LSB) to K3 (MSB) : Data of the number of display digits (4 bits: 16 digits worth)

[Relation between data to be set and the number of digits of COM to be controlled]

HEX	K0	K1	K2	K3	No. of digits of COM	HEX	K0	K1	K2	K3	No. of digits of COM
0	0	0	0	0	COM1-16	8	0	0	0	1	COM1-8
1	1	0	0	0	COM1	9	1	0	0	1	COM1-9
2	0	1	0	0	COM1-2	A	0	1	0	1	COM1-10
3	1	1	0	0	COM1-3	B	1	1	0	1	COM1-11
4	0	0	1	0	COM1-4	C	0	0	1	1	COM1-12
5	1	0	1	0	COM1-5	D	1	0	1	1	COM1-13
6	0	1	1	0	COM1-6	E	0	1	1	1	COM1-14
7	1	1	1	0	COM1-7	F	1	1	1	1	COM1-15

* The state when power is turned on or when the RESET signal is input.

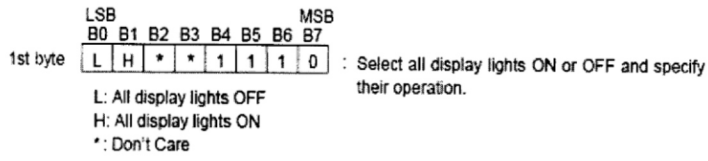
(HCS-12SS59T,Rev1,22-Apr-2009)

6. "All display lights ON" and "All display lights OFF" commands
(Turns the entire display ON and OFF, respectively.)

All display lights ON is used primarily for display testing.

All display lights OFF is primarily used for display blink and to prevent false display upon power-on.

[Command format]



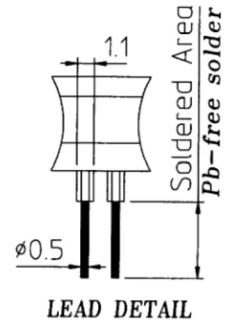
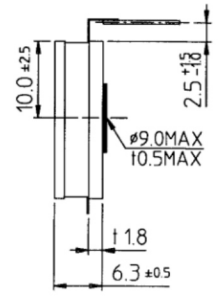
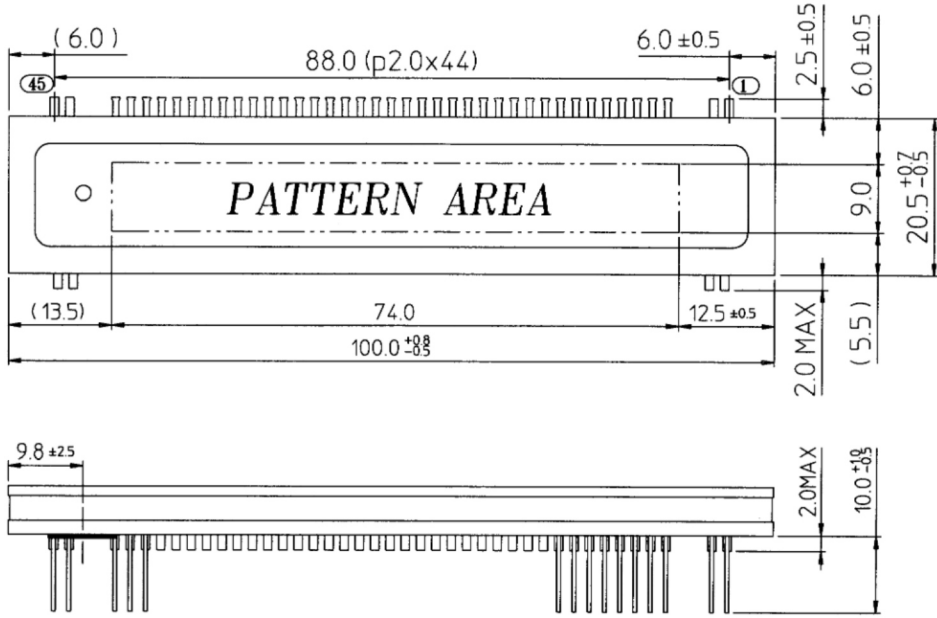
[Data to be setup and display state of SEG and AD]

L	H	Display state of SEG and AD	
0	0	Normal display	
1	0	Sets all outputs to Low	* The state when power is turned on or when $\overline{\text{RESET}}$ signal is input
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	* Priority is given to the All display lights ON command.

16 Segment design								14 Segment design				7 Segment design	
MSEG LSEG	0000	0001	0010	0011	0100	0101	0110	0111	0001	0010	0011	0100	0111
0000	RAM0												
0001	RAM1												
0010	RAM2												
0011	RAM3												
0100	RAM4												
0101	RAM5												
0110	RAM6												
0111	RAM7												
1000	RAM8												
1001	RAM9												
1010	RAMA												
1011	RAMB												
1100	RAMC												
1101	RAMD												
1110	RAME												
1111	RAMF												

16 Segment	14 Segment	7 Segment

OUTER DIMENSIONS



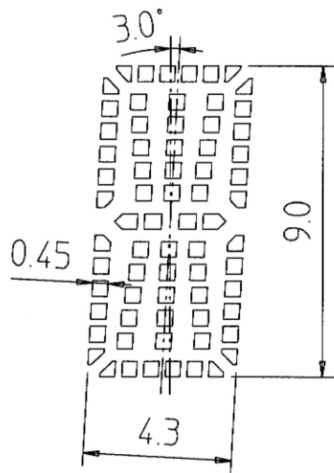
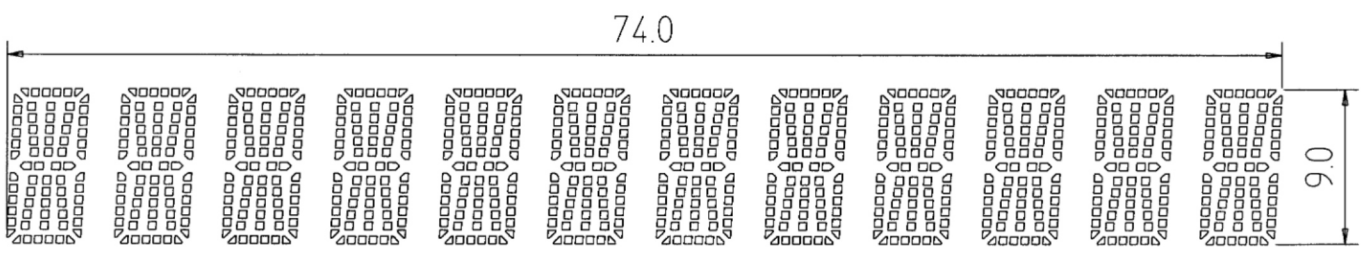
PIN CONNECTION

PIN NO.	45	44	43	42	41	40	39	38~13	12	11	10	9	8	7	6	5	4	3	2	1
CONNECTION	F+	F+	NP	NP	NC	NC	NC	NX	DIN	CLK	CS	RST	OSCO	GND	VDISP	VDDI	NP	NP	F-	F-

- Note ●
- 1) F+, - : Filament pin
- 2) NX : No Extended pin
- 3) NC : No Connection pin
- 4) NP : No pin
- 5) TEST : Open if not use

MODEL : HCS-12SS59T
 OUTER DIMENSIONS
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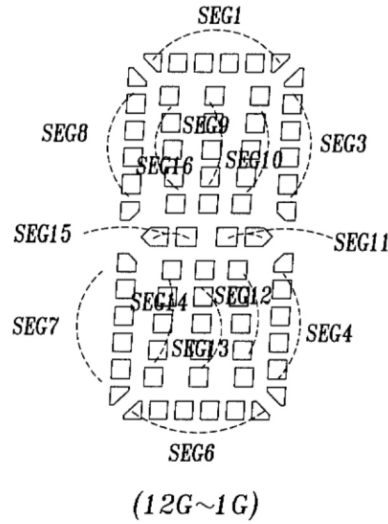
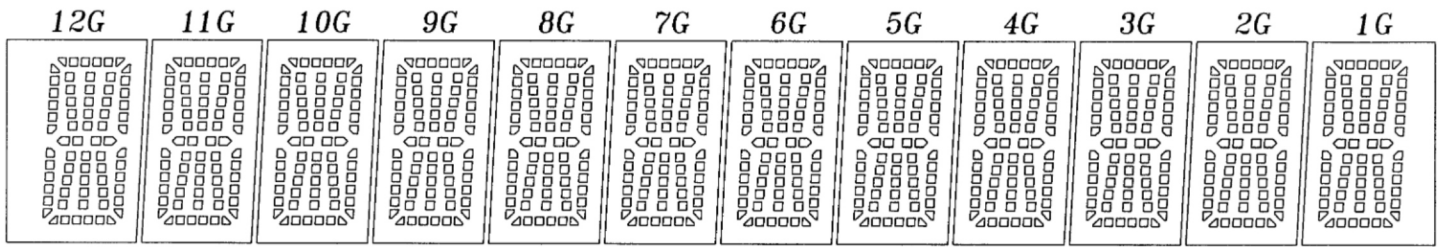
PATTERN DETAILS



◎ Color of Illumination ◎
 · Green (G. x=0.250, y=0.439) ----- All Patterns.

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 PATTERN DETAILS
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GRID ASSIGNMENT



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 GRID ASSIGNMENT
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ANODE CONNECTION

	COM2	COM11	COM10	COM9	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1
	12G	11G	10G	9G	8G	7G	6G	5G	4G	3G	2G	1G
SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1
SEG2												
SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3
SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4
SEG5												
SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6
SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7
SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8
SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9
SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10
SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11
SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12
SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13
SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14
SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15
SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16

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 ANODE CONNECTION
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