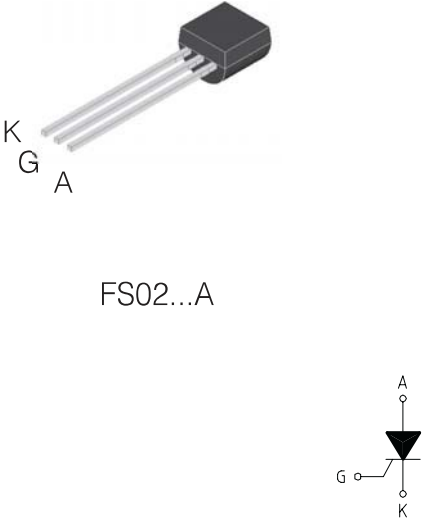


**SENSITIVE GATE SCR**

<p style="text-align: center;">TO92 (Plastic)</p>  <p style="text-align: center;">FS02...A</p>	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center; width: 50%;"><b>On-State Current</b></td> <td style="text-align: center; width: 50%;"><b>Gate Trigger Current</b></td> </tr> <tr> <td style="text-align: center;">1.25 Amp</td> <td style="text-align: center;">&lt; 200 <math>\mu</math>A</td> </tr> <tr> <td colspan="2" style="text-align: center;"><b>Off-State Voltage</b></td> </tr> <tr> <td colspan="2" style="text-align: center;">200 V ÷ 800 V</td> </tr> </table> <p>This series of <b>Silicon C</b>ontrolled <b>R</b>ectifiers uses a high performance PNPN technology.</p> <p>This part is intended for general purpose applications where high gate sensitivity is required.</p>	<b>On-State Current</b>	<b>Gate Trigger Current</b>	1.25 Amp	< 200 $\mu$ A	<b>Off-State Voltage</b>		200 V ÷ 800 V	
<b>On-State Current</b>	<b>Gate Trigger Current</b>								
1.25 Amp	< 200 $\mu$ A								
<b>Off-State Voltage</b>									
200 V ÷ 800 V									

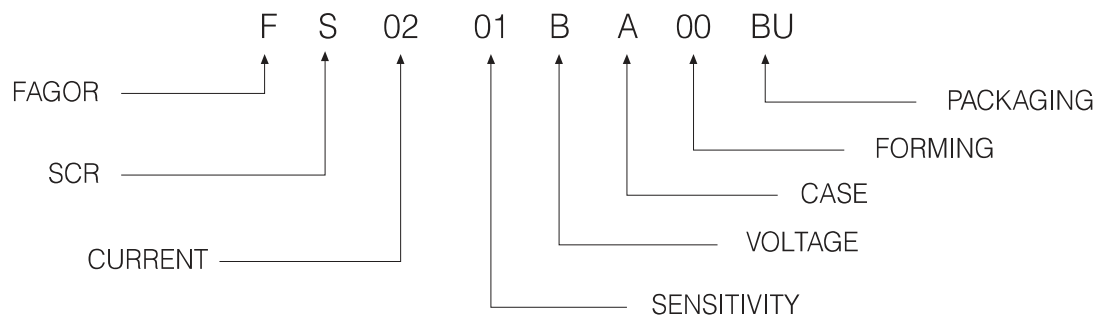
**Absolute Maximum Ratings, according to IEC publication No. 134**

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	On-state Current	180° Conduction Angle, $T_c = 115^\circ C$	1.25	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, $\Theta = 180^\circ$ , $T_c = 115^\circ C$	0.8	A
$I_{TSM}$	Non-repetitive On-State Current	Half Cycle, 60 Hz	25	A
$I_{TSM}$	Non-repetitive On-State Current	Half Cycle, 50 Hz	22.5	A
$I^2t$	Fusing Current	$t_p = 10ms$ , Half Cycle	2.5	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	20 $\mu$ s max.	1.2	A
$P_{GM}$	Peak Gate Dissipation	20 $\mu$ s max.	3	W
$P_{G(AV)}$	Gate Dissipation	20ms max.	0.2	W
$T_j$	Operating Temperature		(-40 to +125)	°C
$T_{stg}$	Storage Temperature		(-40 to +150)	°C
$T_{sld}$	Soldering Temperature	10s max.	260	°C

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE				Unit
			B	D	M	N	
$V_{DRM}$ $V_{RRM}$	Repetitive Peak Off State Voltage	$R_{GK} = 1 k\Omega$	200	400	600	800	V

**SENSITIVE GATE SCR**
**Electrical Characteristics**

SYMBOL	PARAMETER	CONDITIONS	SENSITIVITY				Uni	
			01	02	03	04		
$I_{GT}$	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MIN	1		20	15	$\mu A$
			MAX	20	200	200	50	
$V_{GT}$	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 140\Omega, T_j = 25^\circ C$	MAX	0.8				V
$V_{GD}$	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3k\Omega, R_{GK} = 220\Omega, T_j = 125^\circ C$	MIN	0.1				V
$V_{RGM}$	Reverse Gate Voltage	$I_{RG} = 10\mu A,$	MIN	8				V
$I_H$	Holding Current	$I_T = 50 mA, R_{GK} = 1k\Omega, T_j = 25^\circ C$	MAX	5				mA
$I_L$	Latching Current	$I_G = 1 mA, R_{GK} = 1k\Omega$	MAX	6				mA
$dV / dt$	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, R_{GK} = 1k\Omega, T_j = 125^\circ C$	MIN	15	10	30	30	V/ $\mu s$
$dI / dt$	Critical Rate of Current Rise	$I_G = 2 \times I_{GT}, tr \leq 100 ns, f = 60 Hz, T_j = 125^\circ C$	MIN	50				A/ $\mu s$
$V_{TM}$	On-state Voltage	at $I_T = 2.5 Amp, tp = 380 \mu s, T_j = 25^\circ C$	MAX	1.45	2	1.45		V
$V_{t0}$	Threshold Voltage	$T_j = 125^\circ C$	MAX	0.95				V
$r_d$	Dynamic resistance	$T_j = 125^\circ C$	MAX	400				m $\Omega$
$I_{DRM} / I_{RRM}$	Off-State Leakage Current	$V_D = V_{DRM}, R_{GK} = 1k\Omega, T_j = 125^\circ C$ $V_R = V_{RRM}, T_j = 25^\circ C$	MAX	500				$\mu A$
			MAX	5				$\mu A$
$R_{th(j-c)}$	Thermal Resistance Junction-Case for DC	for AC 360° conduction angle		60				°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S = 1 cm^2$		150				°C/W

**PART NUMBER INFORMATION**


## SENSITIVE GATE SCR

Fig. 1: Maximum average power dissipation versus average on-state current

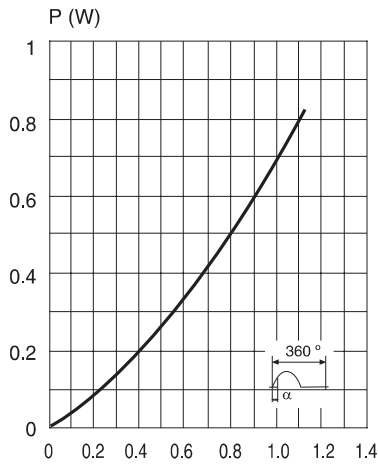


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration

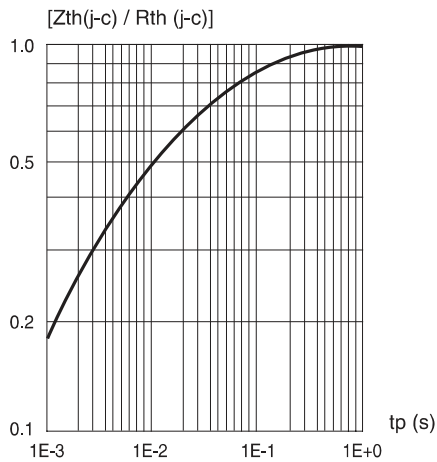


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

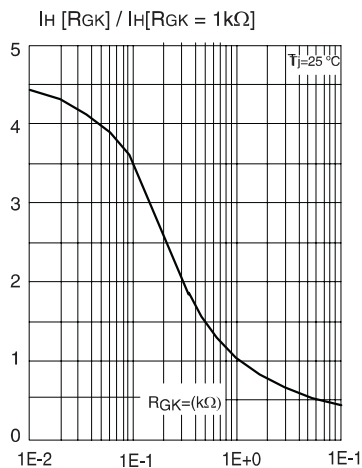


Fig. 2: Average and D.C. on-state current versus case temperature

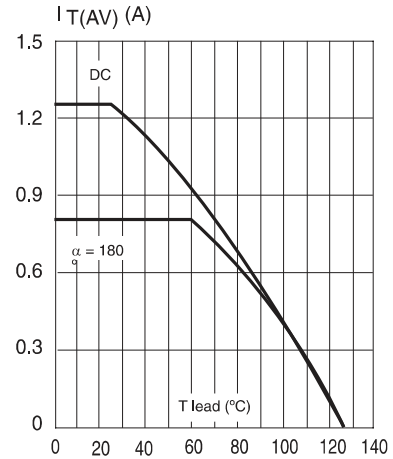


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature

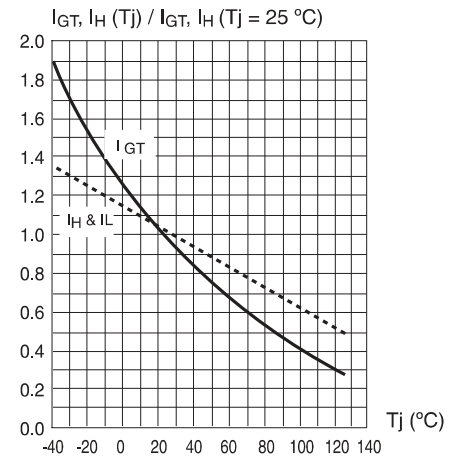
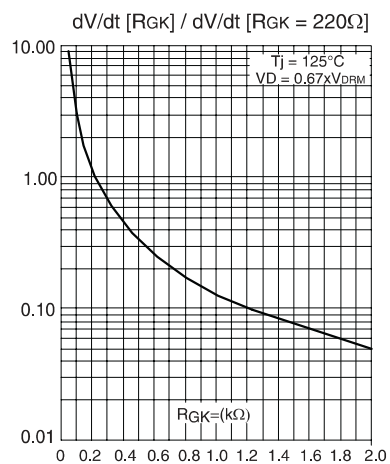


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).



## SENSITIVE GATE SCR

Fig. 7: Relative variation of  $dV/dt$  immunity versus gate-cathode resistance (typical values).

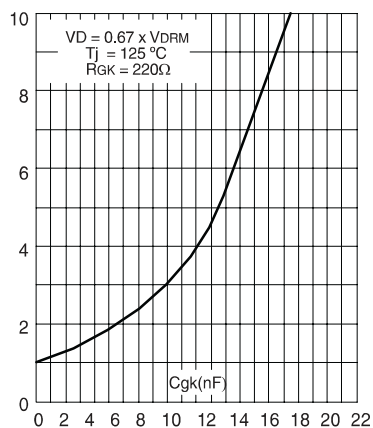


Fig. 9: Non repetitive surge peak on-state current for a sinusoidal pulse with width:  $t_p < 10$  ms, and corresponding value of  $I^2t$ .

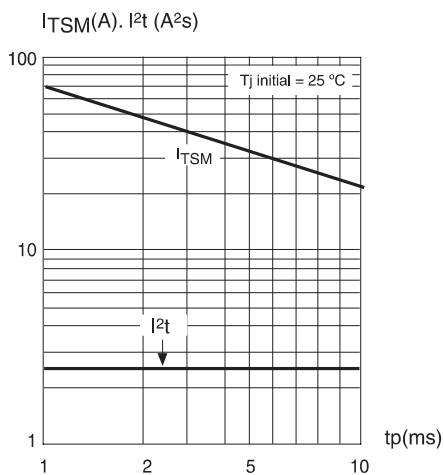


Fig. 8: Non repetitive surge peak on-state current versus number of cycles.

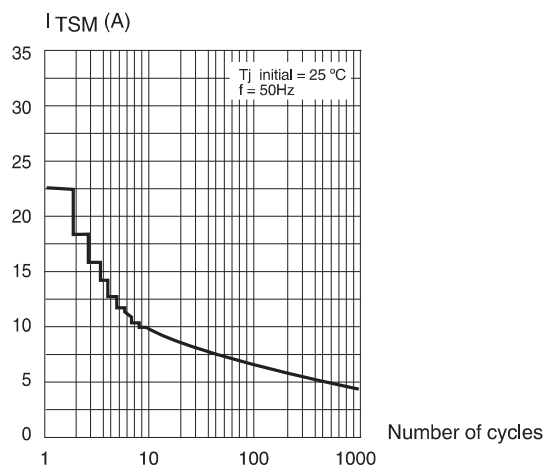
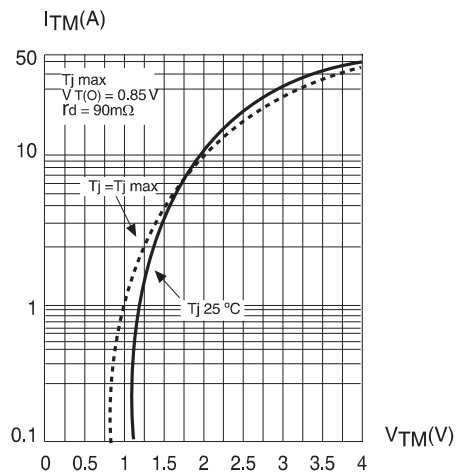


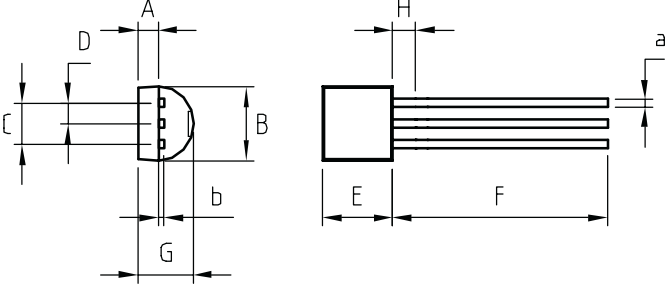
Fig. 10: On-state characteristics (maximum values)



**SENSITIVE GATE SCR**

**PACKAGE MECHANICAL DATA**

TO92

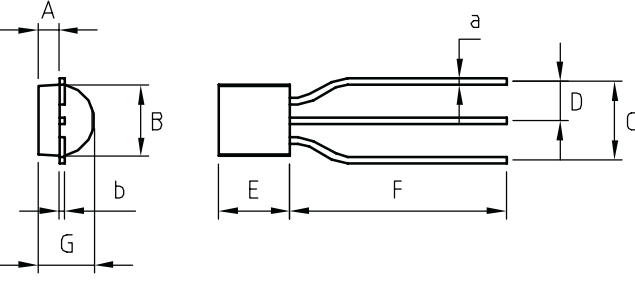


REF.	DIMENSIONS		
	Milimeters		
	Min.	Typ.	Max.
A	0.9	1.2	1.5
B	4.40	4.6	4.80
C	2.34	2.54	2.74
D	1.07	1.27	1.47
E	4.40	4.6	4.80
F	12.7	14.1	15.5
G	3.40	3.6	3.86
H	1.30	1.5	1.70
a	0.38	0.44	0.51
b	0.33	0.41	0.51

Marking: type number  
Weight: 0.2 g

**PACKAGE MECHANICAL DATA**

TO92 (FOR TAPE & REEL)



REF.	DIMENSIONS		
	Milimeters		
	Min.	Typ.	Max.
A	-	1.5	-
B	4.55	4.6	4.65
C	4.96	5.08	5.2
D	2.42	2.54	2.66
E	4.55	4.6	4.65
F	12.7	14.1	15.5
G	3.55	3.6	3.65
a	0.38	0.43	0.48
b	0.33	0.38	0.43

Marking: type number  
Weight: 0.2 g